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| EXAMINER | |
|---|---|
| GEBREMARIAM, SAMUEL A | |
| ART UNIT | PAPER NUMBER |
| 2811 | |

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/768,185 | ITO, TOSHIO | |
| | Examiner | Art Unit | |
| | Samuel A Gebremariam | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/24/04, 2/2/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what applicant is trying to claim when stating "a top surface of the dielectric layer is substantially coplanar with aligned a top surface of the projecting portion" as recited in claim 4. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-3, 5-10, and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Basceri et al, US patent No. 6,444,478.

Regarding claim 1, Basceri teaches (figs. 1 and 2) a ferroelectric capacitor (31) comprising: a bottom electrode (32) which has a plate portion (lower portion of 32) and a projecting portion (upper portion of 32), wherein the projecting portion is arranged on a central area of the plate portion; a dielectric layer (14) formed on a peripheral area (upper surface of bottom electrode 32) of the bottom electrode (32); a ferroelectric layer (16) formed on the dielectric layer (14) and on the projection portion of the bottom electrode; and a top electrode (36) formed on the ferroelectric layer (16).

Regarding claim 2, Basceri teaches the entire claimed structure of claim 1 above including the ferroelectric layer includes a damaged area, which is formed on the dielectric layer. Basceri teaches patterned layers (fig. 2) where the sides of the layers that are aligned. APA teaches (page 2) that etching of the bottom electrode, ferroelectric layer and the top electrode would cause damage on the ferroelectric dielectric layer. Therefore Basceri inherently teaches a damaged ferroelectric layer.

Regarding claim 3, Basceri teaches the entire claimed structure of claim 1 above including the bottom electrode (32) comprises the plate portion and the projecting portion as single unitary electrode (refer to fig. 2).

Regarding claim 5, Basceri teaches the entire claimed structure of claim 1 above including a side surface of the plate portion of the bottom electrode, a side surface of the dielectric layer, a side surface of the ferroelectric layer and a side surface of the top electrode are aligned (refer to fig. 4).

Regarding claim 6, Basceri teaches the entire claimed structure of claim 1 above including the bottom electrode and the top electrode are made of an oxidation resistance metal or a conductive metal oxide (col. 14, lines 14-21 and lines 61-67).

Regarding claim 7, Basceri teaches the entire claimed structure of claim 1 above including the plate portion of the bottom electrode and the projection portion of the bottom electrode are made of different material (col. 14, lines 14-21). Basceri teaches the bottom electrode may be formed from 1 or more metal layers as in col. 14, lines 14-21.

Regarding claim 8, Basceri teaches the entire claimed structure of claims 1 and 8 above including the plate portion of the bottom electrode includes a lower layer and an upper layer (lower portion of the bottom electrode further have a lower layer and an upper layer).

Regarding claim 9, Basceri teaches the entire claimed structure of claims 1 and 7 above including the projection portion of the bottom electrode is made of platinum (col. 14, lines 14-21).

Regarding claims 10 and 13, Basceri teaches (figs. 1 and 2) the entire claimed structure of claims 1 and 5 above including a ferroelectric capacitor comprising: a bottom electrode (32); a top electrode (36); a ferroelectric layer (31) formed between the bottom electrode and the top electrode; and a dielectric spacer (14) formed between the bottom electrode (32) and the top electrode (36), wherein the dielectric spacer decreases an electric field strength at a peripheral area of the capacitor.

Regarding claim 14 and 15, Basceri teaches (figs. 1 and 2) the entire claimed structure of claims 1 and 5 above including a spacer layer (14) formed on a peripheral area (upper portion of 32) of the first electrode; a ferroelectric layer (16) formed on the dielectric spacer and on the projecting portion (upper portion of 32); and a second electrode (36) formed on the ferroelectric layer.

5. Claims 1, 4, 11 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Natori et al, US patent No. 6,459,111.

Regarding claim 1 Natori teaches (fig. 3) a ferroelectric capacitor comprising: a bottom electrode (39) which has a plate portion (lower portion of 39) and a projecting portion (upper portion of 39), wherein the projecting portion is arranged on a central area of the plate portion; a dielectric layer (40) formed on a peripheral area of the bottom electrode (39); a ferroelectric layer (42) formed on the dielectric layer (40) and on the projection portion of the bottom electrode; and a top electrode (43) formed on the ferroelectric layer (42).

Regarding claim 4, Natori teaches the entire claimed structure of claim 1 above including a top surface of the dielectric layer is substantially coplanar (portion of 40 that is coplanar with 39) and aligned with a top surface of the projecting portion (upper portion of 39, refer to fig. 3).

Regarding claim 11, Natori teaches the entire claimed structure of claim 1 above including the bottom electrode (39) includes a projecting portion (top portion of 39) arranged at a central area of the bottom electrode, and wherein the dielectric spacer is arranged around the projecting portion (layer 40 is formed around 39).

Regarding claim 12, Natori teaches the entire claimed structure of claim 1 above including a distance between the bottom electrode (39) and the top electrode (43) at a peripheral area of the capacitor is grater than a distance between the bottom electrode and the top electrode at a central area of the capacitor. The distance between the top electrode and the bottom electrode taken at the base of the bottom electrode is greater than the distance between the top electrode and the bottom electrode taken at the top of the bottom electrode.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Natori et al. in view of Eguchi US patent No. 6,093,575.

Regarding claim 16, Natori teaches (fig. 3); a ferroelectric capacitor formed on a top surface of the insulating layer (31) (fig. 3C), the ferroelectric capacitor including a bottom electrode (39) formed on the insulating layer (31), the bottom electrode having a plate portion (lower portion of 39) and a projecting portion (upper portion of 39), wherein the projecting portion is arranged on a central area of the plate portion, a dielectric layer (40) formed on the peripheral area of the bottom electrode (39), a ferroelectric layer (42) formed on the dielectric layer (40) and on the projecting portion, and a top electrode

(43) formed on the ferroelectric layer; and a plug electrode (32) which is embedded in the insulating layer (31).

Natori does not explicitly teach a semiconductor device comprising: a semiconductor substrate; a transistor formed on the semiconductor substrate, the transistor having a source region, a drain region and a gate electrode; an insulating layer formed on the semiconductor substrate and the transistor and the plug electrode connects the source region of the switching transistor to the bottom electrode of the ferroelectric capacitor.

Eguchi teaches (fig. 2C) a semiconductor substrate (1); a transistor (9) formed on the semiconductor substrate, the transistor having a source region (8a), a drain region (8b) and a gate electrode (4); an insulating layer (10) formed on the semiconductor substrate (1) and the transistor (9) and plug electrode (part electrode 22 connecting to region 8a) connects the source region (8a) of the transistor to the bottom electrode of the ferroelectric capacitor. Furthermore Eguchi teaches a MOS transistor that is capable of performing as a switching transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the transistor connection portion taught by Eguchi in the structure of Natori in order to integrate the ferroelectric capacitor with other portion of the integrated device.

Regarding claim 17, Natori teaches substantially the entire claimed structure of claim 16 above including the top surface of the insulating layer (40) is formed

substantially flat (refer to fig. 3, layer 40 has a flat surface on the periphery and the middle).

Regarding claim 18, Natori teaches substantially the entire claimed structure of claim 16 above including the ferroelectric capacitor is located over the source region of the switching transistor.

7. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Natori et al. in view of Kobayashi US patent No. 6,495,879.

Regarding claim 19, Natori teaches (fig. 3); a ferroelectric capacitor formed on a top surface of the insulating layer (31) (fig. 3C), the ferroelectric capacitor including a bottom electrode (39) formed on the insulating layer (31), the bottom electrode having a plate portion (lower portion of 39) and a projecting portion (upper portion of 39), wherein the projecting portion is arranged on a central area of the plate portion, a dielectric layer (40) formed on the peripheral area of the bottom electrode (39), a ferroelectric layer (42) formed on the dielectric layer (40) and on the projecting portion, and a top electrode (43) formed on the ferroelectric layer; and a plug electrode (32) which is embedded in the insulating layer (31).

Kobayashi teaches (figs. 10A-10F) a semiconductor substrate (11); a transistor (col. 9, lines 34-41) formed on the semiconductor substrate (11), the transistor having a source region (source/drain regions 18), and a gate electrode (17); an insulating layer (col. 9, lines 34-41) formed on the semiconductor substrate (11) and a top electrode (15) formed on a ferroelectric layer (14); and a wiring (16) which connects the source region (18) of the transistor to the top electrode (15) of the ferroelectric capacitor (25)

(refer to fig. 10F). Furthermore Kobayashi teaches a MOS transistor that is capable of performing as a switching transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the transistor connection portion taught by Kobayashi in the structure of Natori in order to integrate the ferroelectric capacitor with other portion of the integrated device.

Regarding claim 20, Natori teaches substantially the entire claimed structure of claim 19 above including the wiring (16, portion of 16 inside the via) includes a plug portion which extends from the source region (18) of the switching transistor to the top surface of the insulating layer (26) and a wiring portion (portion of 16 that connects to 15) which connects a top of the plug to the top electrode (15) of the ferroelectric capacitor (25).

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D and E are cited as being related to capacitors. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
December 12, 2004

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